



YEAR 12 A LEVEL COMPUTER SCIENCE AUTUMN TERM 1 – PAPER 1

'An ambitious curriculum that meets the needs of all'

Medium Term Planning – Components of a Computer

Curriculum Intent	Pupils will be taught the following National Curriculum guidelines this term:
Skills/Assessment Objective Links	<p>At the end of this Unit all students should be able to:</p> <ul style="list-style-type: none">List the basic internal components of the processor: ALU, Control Unit, registers and busesName the different registers used in the Fetch-Decode-Execute cycleList factors which affect the performance of the CPU: clock speed, number of cores, cacheExplain what is meant by a multicore system and parallel processingDescribe the uses of RAM, ROM and virtual storageDescribe typical uses of magnetic, flash and optical storage devices <p>Most students will be able to:</p> <ul style="list-style-type: none">Describe the Fetch-Decode-Execute cycle and its effect on registersDescribe the role of the data, address and control busesDescribe the use of pipelining in a processor to improve efficiencyDescribe von Neumann and Harvard architectures and the advantages and use of eachDescribe the characteristics and use of a Graphics Processing Unit (GPU)Describe the benefits and potential problems of virtual storageDescribe the uses of magnetic, flash and optical storage devicesDescribe how different I/O and storage devices can be applied to the solution of different problems <p>Some students will be able to:</p> <ul style="list-style-type: none">Describe features of contemporary processor architectureDescribe the differences between, and uses of, CISC and RISC architectureExplain how system architecture and bus width relates to assembly language programs
Numeracy	Clock speed, number of cores, cache, ALU
Literacy	<p>Vocabulary Tier 3: Arithmetic and Logic Unit (ALU), Control Unit, bus, registers, program counter (PC), accumulator (ACC), memory address register (MAR), memory data register (MDR), current instruction register (CIR), Fetch-Decode-Execute cycle, clock speed, core, cache, pipelining, von Neumann architecture, Harvard architecture, CISC, RISC, multicore, parallel systems, graphics processing unit (GPU) magnetic, flash and optical storage devices, RAM, ROM, virtual storage</p> <p>Vocabulary Tier 2: storage, control, clock, speed,</p> <p>Reading: Worksheets, presentations, answer sheets, exam questions, mark scheme, further reading for homework</p> <p>Writing: Answer on the worksheet via word</p> <p>Oracy: listening and using tier 3 words</p>
Becoming future ready	<p>Careers/Employability:</p> <p>Understand the grade requirements at universities and the topics that can be applied for. Explore apprenticeship opportunities with a range of industries.</p> <ul style="list-style-type: none">Software Architect.Data Scientist.Machine Learning Engineer.Blockchain DeveloperCybersecurity Engineer.Cloud Solutions Architect.AI Research Scientist.Full-Stack Developer.
Adaptation	Throughout this topic, quality first teaching will provide differentiation:

QFT/SEND Provision	<p>By product: Learners are asked to present outcomes in a different way via pieces of writing, targeted questioning, models and drawings and speaking.</p> <p>By resource: Worksheets are well presented and accessible. Instructions are clearly outlined and separate from the information so that pupils know where to begin and end. Handouts are differentiated by outcome. Resources used will appeal to the range of preferred learning styles of pupils e.g. visual, auditory or kinesthetic learners. Scaffolding of tasks – word frames.</p> <p>By Intervention: By providing different levels of supervision and support</p> <p>By Progressive Questioning: Exploring pupils’ understanding through interactive dialogue using Blooms Taxonomy.</p> <p>By Grouping: According to prior attainment, gender, social preference, preferred learning style.</p> <p>By Task: Pupils identify targets which are meaningful to them via feedback sheets</p> <p>By Offering Optional Activities: In class or as homework, to extend learning.</p> <p>This QFT/SEND provision will be explicit within the lesson by lesson schemes of work.</p>
Implementation Curriculum Delivery	To be able to:
Learning Outcomes (Knowledge)	<p>Topic 1 Processor components Describe the function of the ALU and Control Unit Describe the Fetch-Execute cycle and the role of the following registers:</p> <ul style="list-style-type: none"> ○ Program counter ○ Accumulator ○ Memory Address Register ○ Memory Data Register ○ Current Instruction Register <p>Topic 2 Processor Performance Describe the factors affecting the performance of the CPU: clock speed, number of cores, cache Understand the use of pipelining in a processor to improve efficiency</p> <p>Topic 3 Types of Processor Describe von Neumann, Harvard and contemporary processor architecture Describe the differences between, and uses of, CISC and RISC processors Describe GPUs and their uses Describe multicore and parallel systems</p> <p>Topic 4 Input Devices Describe different input devices Explain how different input devices can be applied as a solution to different problems</p> <p>End of unit assessment</p>
Current learning to be developed in the future within:	Links to software and networks
Assessment	See assessment maps for formative and summative assessment opportunities.
Impact	<p>Review assessment results and target pupils that require further support via:-</p> <ul style="list-style-type: none"> • Learning conversation • Changing seating plan • Plan lessons to address areas of concern in assessment • Targeted homework based on low performance areas identified in the assessment and marked pieces • Stretch and challenge high ability pupils by identifying ambitious next steps to expand knowledge <p>Create a feedback sheet for each student Each student identifies areas of Green, Amber and Red using Mark Assessment on their feedback sheet Complete NOW task on areas identified as Amber and Red</p>

