



# YEAR 13 A LEVEL COMPUTER SCIENCE SPRING 2<sup>nd</sup> TERM 2 – PAPER 1

'An ambitious curriculum that meets the needs of all'

## Medium Term Planning – Boolean Algebra

Curriculum Intent	Pupils will be taught the following National Curriculum guidelines this term:
Skills/Assessment Objective Links	<p><b>At the end of this Unit all students should be able to:</b></p> <ul style="list-style-type: none"><li>construct truth tables for a variety of logic gates</li><li>draw and interpret logic gate circuit diagrams involving multiple gates</li><li>write a Boolean expression for a given logic gate circuit</li><li>draw an equivalent logic gate circuit for a given Boolean expression</li><li>Draw a Karnaugh map corresponding to a given expression or truth table</li><li>Draw a truth table for a half adder</li><li>State what a D type flip flop is and what it is used for</li></ul> <p><b>Most students will be able to:</b></p> <ul style="list-style-type: none"><li>Complete a truth table for a given logic gate circuit</li><li>Represent and solve a problem using Boolean logic</li><li>Use de Morgan's laws to manipulate and simplify Boolean expressions</li><li>Simplify an expression using a Karnaugh map</li><li>Draw the logic circuit for a half adder</li><li>Give the output from a series of connected D type flip flops</li></ul> <p><b>Some students will be able to:</b></p> <ul style="list-style-type: none"><li>Draw the logic circuit for a full adder</li><li>Explain the logic associated with D type flip flops</li></ul>
Numeracy	Logic gates, Truth tables, Boolean algebra
Literacy	<p><b>Vocabulary Tier 3:</b> logic gate, truth table, Boolean algebra, distribution, association, commutation, double negation, Karnaugh map, D type flip flop, half adder, full adder</p> <p><b>Vocabulary Tier 2:</b> logic</p> <p><b>Reading:</b> Worksheets, presentations, answer sheets, exam questions, mark scheme, further reading for homework</p> <p><b>Writing:</b> Answer on the worksheet via word</p> <p><b>Oracy:</b> listening and using tier 3 words</p>
Becoming future ready	<p><b>Careers/Employability:</b></p> <p>Understand the grade requirements at universities and the topics that can be applied for. Explore apprenticeship opportunities with a range of industries.</p> <ul style="list-style-type: none"><li>Software Architect.</li><li>Data Scientist.</li><li>Machine Learning Engineer.</li><li>Blockchain Developer</li><li>Cybersecurity Engineer.</li><li>Cloud Solutions Architect.</li><li>AI Research Scientist.</li><li>Full-Stack Developer.</li></ul>
Adaptation	Throughout this topic, quality first teaching will provide differentiation:
QFT/SEND Provision	<p><b>By product:</b> Learners are asked to present outcomes in a different way via pieces of writing, targeted questioning, models and drawings and speaking.</p> <p><b>By resource:</b> Worksheets are well presented and accessible. Instructions are clearly outlined and separate from the information so that pupils know where to begin and end. Handouts are differentiated by outcome. Resources used will appeal to the range of preferred learning styles of pupils e.g. visual, auditory or kinesthetic learners. Scaffolding of tasks – word frames.</p> <p><b>By Intervention:</b> By providing different levels of supervision and support</p>



**By Progressive Questioning:** Exploring pupils' understanding through interactive dialogue Blooms Taxonomy.  
**By Grouping:** According to prior attainment, gender, social preference, preferred learning style  
**By Task:** Pupils identify targets which are meaningful to them via feedback sheets  
**By Offering Optional Activities:** In class or as homework, to extend learning.  
This QFT/SEND provision will be explicit within the lesson by lesson schemes of work.

**Implementation  
Curriculum Delivery**

To be able to:

**Learning Outcomes  
(Knowledge)**

**Topic 1 Logic Gates**

Construct a truth table for a variety of logic gates  
Be familiar with drawing and interpreting logic gate circuit diagrams involving multiple gates  
Complete a truth table for a given logic gate circuit  
Write a Boolean expression for a given logic gate circuit  
Draw an equivalent logic gate circuit for a given Boolean expression

**Topic 2 Simplifying Boolean expressions**

Be familiar with the use of Boolean identities and De Morgan's laws to manipulate and simplify Boolean expressions  
Write a Boolean expression for a given logic gate circuit, and vice versa

**Topic 3 Karnaugh map**

Understand the correspondence between a truth table and a Karnaugh map  
Understand how to fill out a Karnaugh map for a given expression  
Understand how to group items in a Karnaugh map  
Interpret the groupings in a Karnaugh map  
Simplify Boolean expressions with two, three or four variables using a Karnaugh map

**Topic 4 Adders and D type flip flops**

Recognise and trace the logic of the circuits of a half adder and a full adder  
Construct the circuit for a half adder  
Understand the logic associated with D type flip flops

End of unit assessment

**Current learning to  
be developed in the  
future within:**

**Assessment**

See assessment maps for formative and summative assessment opportunities.

**Impact**

Review assessment results and target pupils that require further support via:-

- Learning conversation
- Changing seating plan
- Plan lessons to address areas of concern in assessment
- Targeted homework based on low performance areas identified in the assessment and marked pieces
- Stretch and challenge high ability pupils by identifying ambitious next steps to expand knowledge

Create a feedback sheet for each student

Each student identifies areas of Green, Amber and Red using Mark Assessment on their feedback sheet

Complete NOW task on areas identified as Amber and Red